

AMENDMENTS TO THE DRAWINGS

The attached sheets of drawings includes changes to Figures 1e and 2e.

Attachment: Replacement sheet
 Annotated sheet showing changes

REMARKS

Claims 20-38 are pending. Claims 20-37 stand rejected and claim 38 is withdrawn from consideration. By this Amendment, claims 20 and 35 have been amended. The amendments made to the claims do not alter the scope of these claims, nor have these amendments been made to define over the prior art. Rather, the amendments to the claims have been made to improve the form thereof. In light of the amendments and remarks set forth below, Applicants respectfully submit that each of the pending claims is in immediate condition for allowance.

The Office Action objects to Figures 1e and 2e for not depicting the semiconductor memory element arrangement 100. Applicants have amended Figures 1e and 2e to show semiconductor memory element arrangement 100. Therefore, Applicants respectfully request reconsideration and withdrawal of this rejection.

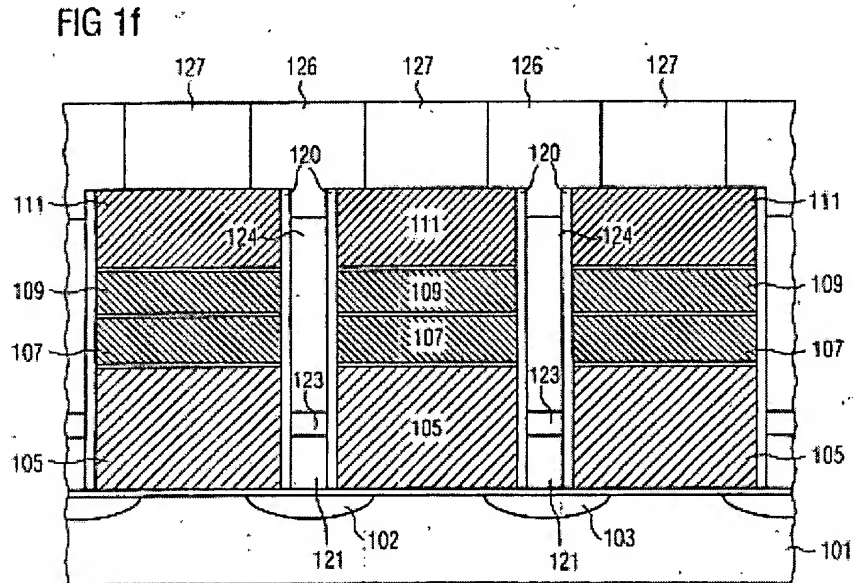
Claims 20-37 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,973,356 ("Noble"). Applicants respectfully request reconsideration and withdrawal of this rejection.

Among the limitations of independent claim 20 and corresponding claim 37 not present in Noble is forming a layer system, including a floating gate and a multiple tunnel barrier arrangement formed on the floating gate, on the first insulating layer. Additionally, Applicants note that the first and second gate electrodes are not present in Noble because the explicitly recited layer structure in the claim is not disclosed.

As disclosed in the present specification and shown for example in Fig. 1f, reproduced below, a floating gate 105 and multiple tunnel barrier layers 106-110 form the explicitly claimed layer system. Further, elements 121 and 124 are not shown in Noble. Specifically, as shown in Fig. 1f, electrode 123 is found adjacent to the floating

gate 105 and electrode 124 is found adjacent to the multiple tunnel barrier. This structure and the method for producing it is not taught or suggested in Noble.

Figure 1f From The Present Application



In contrast, in Noble, as shown in Figure 12, reproduced below, a series of layers 500, 505, 515, and 520 are arranged. A gate dielectric 800 is common to all of these layers not one of the layers as recited in the claim and shown in Fig. 1f above. A floating gate structure 1000 is parallel to gate dielectric 800. Finally, control gate 335 is in channel 1200. This structure is unlike the structure formed by the explicitly recited method of claim 20 and thus does not anticipate the pending claims.

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Figure 12 of Noble

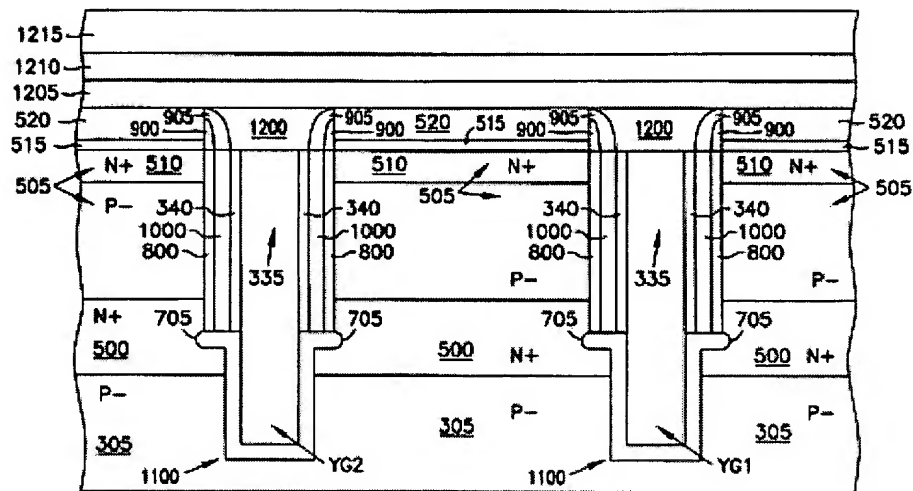


FIG. 12

Because the explicitly recited layer system and first and second gate electrodes are not disclosed in Noble, Applicants respectfully submit that each of claims 20-37 are in immediate condition for allowance.

Applicants have responded to all of the rejections and objections recited in the Office Action. Reconsideration and a Notice of Allowance for all of the pending claims are therefore respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Application No. 10/805,670

Docket No.: V0195.0012

If the Examiner believes an interview would be of assistance, the Examiner is welcome to contact the undersigned at the number listed below.

Dated: December 22, 2006

Respectfully submitted,

By 

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IRB/mgs
Attachments



FIG 1e

100

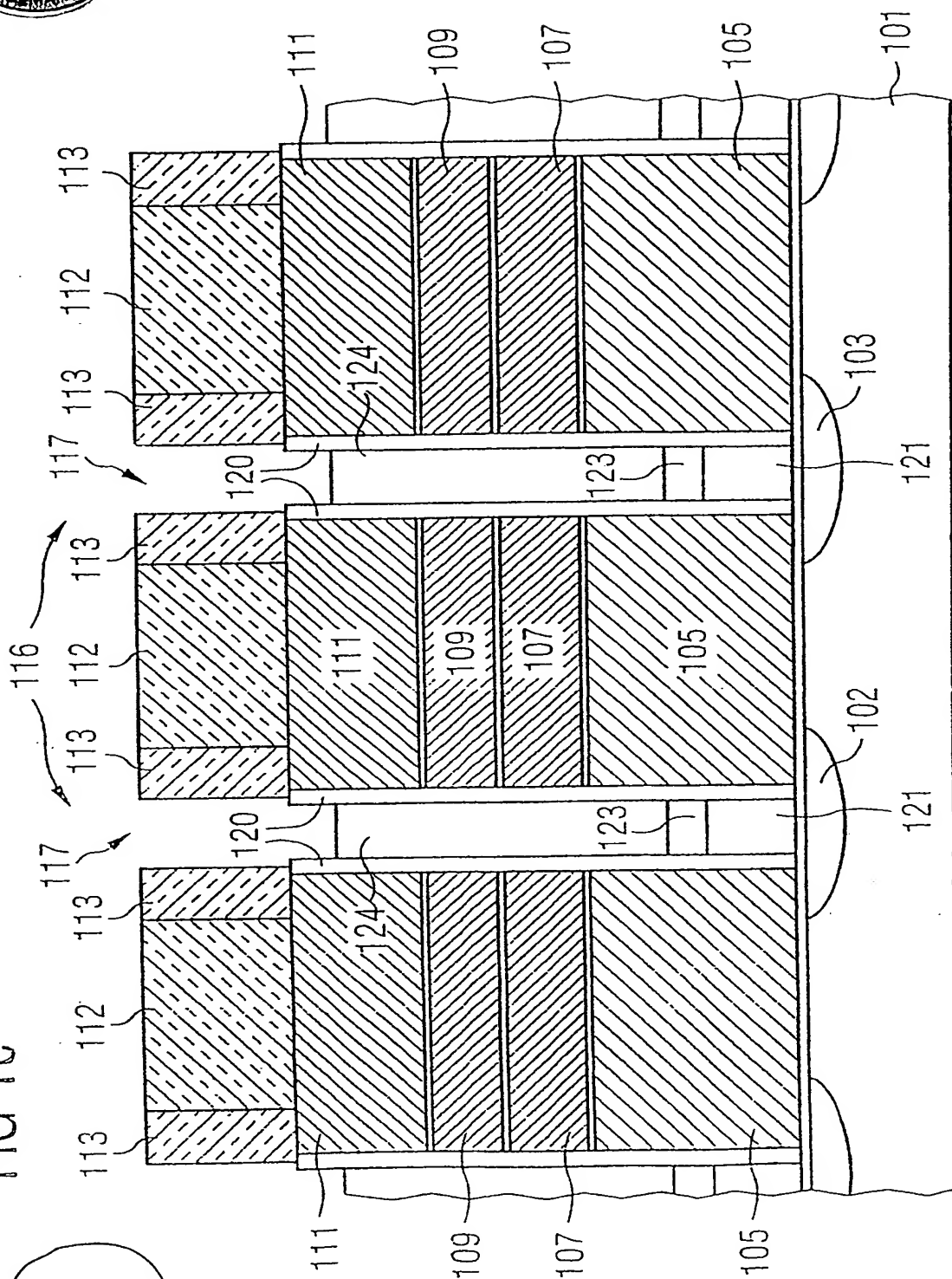




FIG 2e

